The drawing Fig. 4 has been corrected in red to label the dielectric layer 36 first described on page 9 of the Specification. Formal drawings will be sent once the Examiner has approved the drawing changes.

The Specification has been amended to correct an error wherein the shallow trench is referred to as 23 in Fig. 7. The shallow trench in Fig. 7 is labeled 24.

Claims 6-7 and 12-13 have been canceled as the Examiner has found them to be of improper dependent form. Claims 4, 5, 7, and 10 have been amended to overcome rejection under 35 U.S.C. 112, second paragraph. The Examiner is thanked for his very helpful suggestions in this matter.

All Claims are believed to be in condition for Allowance and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-13 as being unpatentable over Kunikiyo in combination with Chen et al and Wolf is requested in view of Amended Claims 1 and 10 and in accordance with the following remarks.

It is important to Applicants' invention that there is no channel stopper implant underneath the partial isolation trench 24. This is because our structure is such that the contact to the substrate silicon is between the partial or shallow trench and the full or deep trench. Kunikiyo forms channel stoppers 125 and 126 underlying the partial trenches 116 (See Fig. 16, col. 16, lines 42-47). Claims 1 and 8 have been amended to make it clear that no implant is made underlying the partial trench.

It is agreed that Chen et al teaches methods of filling trenches and that Wolf teaches a method of forming interlevel dielectrics as well as disclosing conductive materials. However, it is believed that the amendment to the claims makes clear the important difference between Kunikiyo and Applicants' invention. In fact, in comparing his invention to a well-known technique, the presence of the channel stopper under the partial trench is one of the crucial differences (see col. 11, lines 54-67).

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-13 as being unpatentable over Kunikiyo in combination with Chen et al and Wolf is requested in view of Amended Claims 1 and 10 and in accordance with the remarks above.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Foong not find that the Claims are now Allowable that he call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the first full paragraph on page 9 with the following:

Contact openings are etched through the ILD layer 36 to the underlying source/drain regions 32. At the same time, a contact opening is etched through the ILD layer 36 to contact portions of both the shallow trench [23] 24 and a nearby deep trench 29.

IN THE CLAIMS

Please amend the Claims as follows:

1. (AMENDED) A method of forming a silicon-on-insulator device in the fabrication of integrated circuits comprising:

providing a silicon layer overlying an oxide layer on a silicon semiconductor substrate;

etching a first trench into said silicon layer wherein said first trench extends partially through said silicon layer and does not extend to underlying said

oxide layer and wherein no implant is made underlying said first trench;

filling said first trench with an insulating layer;

etching second trenches into said silicon layer wherein said second trenches extend fully through said silicon layer to underlying said oxide layer and wherein said second trenches separate active areas of said semiconductor substrate and wherein one said first trenches lies within each of said active areas;

filling said second trenches with an insulating layer;

thereafter forming gate electrodes and associated source and drain regions in and on said silicon layer between said second trenches;

depositing an interlevel dielectric layer overlying said gate electrodes;

opening first contacts through said interlevel dielectric layer to underlying said source and drain regions and opening a second contact opening through said interlevel dielectric layer in each of said active regions wherein said second contact opening contacts both said first trench and one of said second trenches; and

filling said first and second contact openings with a conducting layer to complete formation of said

silicon-on-insulator device in said fabrication of integrated circuits.

4. (AMENDED) The method according to Claim 1 wherein said interlevel dielectric layer comprises one of the group [containing] consisting of sub-atmospheric borophosphosilicate glass (BPSG), tetraethoxysilane (TEOS) oxide, fluorinated silicate glass (FSG), and low dielectric constant dielectric materials and has a thickness of between about 6000 and 20,000 Angstroms.

5. (AMENDED) The method according to Claim 1 wherein said conducting layer comprises one of the group [containing] consisting of tungsten and aluminum-copper alloys.

Please cancel Claims 6-7.

8. (AMENDED) A method of forming a silicon-on-insulator device in the fabrication of integrated circuits comprising:

providing a silicon layer overlying an oxide layer on a silicon semiconductor substrate;

etching a first trench into said silicon layer wherein said first trench extends partially through said

silicon layer and does not extend to underlying said oxide layer and wherein said first trench is etched into said silicon layer to a depth of between 1/2 and 3/4 of the thickness of said silicon layer and wherein no implant is made underlying said first trench;

etching second trenches into said silicon layer wherein said second trenches extend fully through said silicon layer to underlying said oxide layer and wherein said second trenches separate active areas of said semiconductor substrate and wherein one said first trench lies within each of said active areas;

filling said first and second trenches with an insulating layer;

thereafter forming gate electrodes and associated source and drain regions in and on said silicon layer between said second trenches;

depositing an interlevel dielectric layer overlying said gate electrodes;

opening first contacts through said interlevel dielectric layer to underlying said source and drain regions and opening a second contact opening through said interlevel dielectric layer in each of said active regions wherein said second contact opening contacts both said first trench and one of said second trenches; and

filling said first and second contact openings with a conducting layer to complete formation of said silicon-on-insulator device in said fabrication of integrated circuits.

10. (AMENDED) The method according to Claim 8 wherein said interlevel dielectric layer comprises one of the group [containing] consisting of sub-atmospheric borophosphosilicate glass (BPSG), tetraethoxysilane (TEOS) oxide, fluorinated silicate glass (FSG), and low dielectric constant dielectric materials and has a thickness of between about 6000 and 20,000 Angstroms.

11. (AMENDED) The method according to Claim 8 wherein said conducting layer comprises one of the group [containing] consisting of tungsten and aluminum-copper alloys.

Please cancel Claims 12-20.

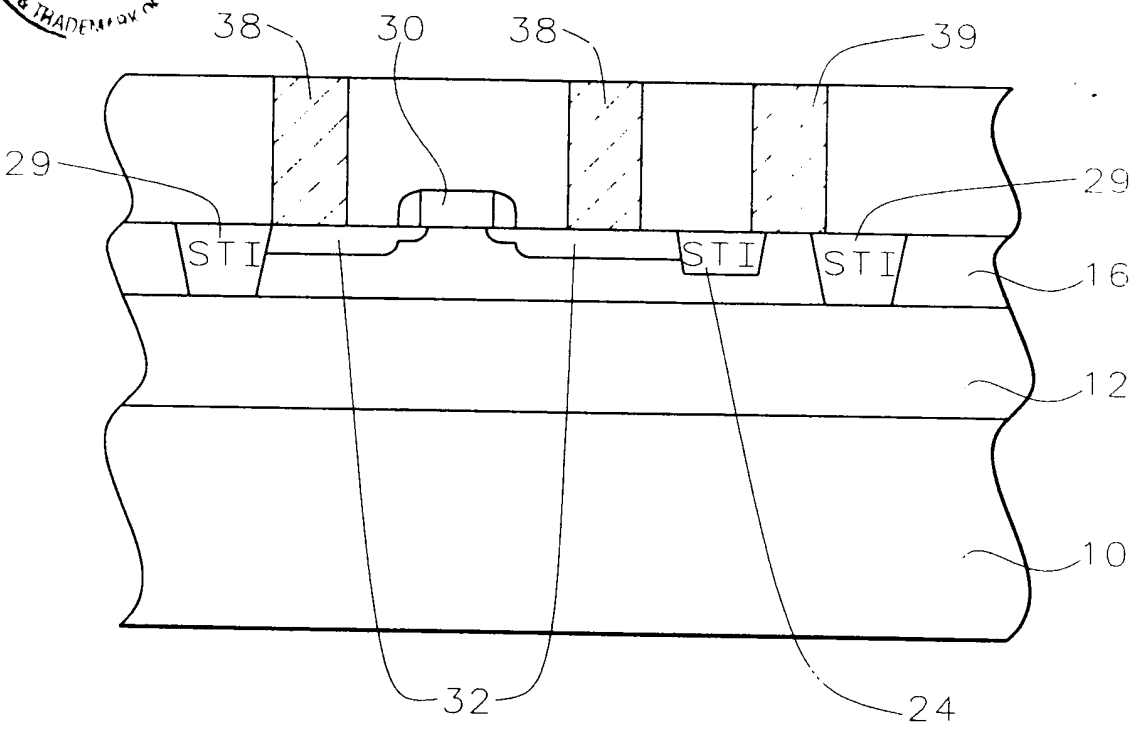

FIG. 7

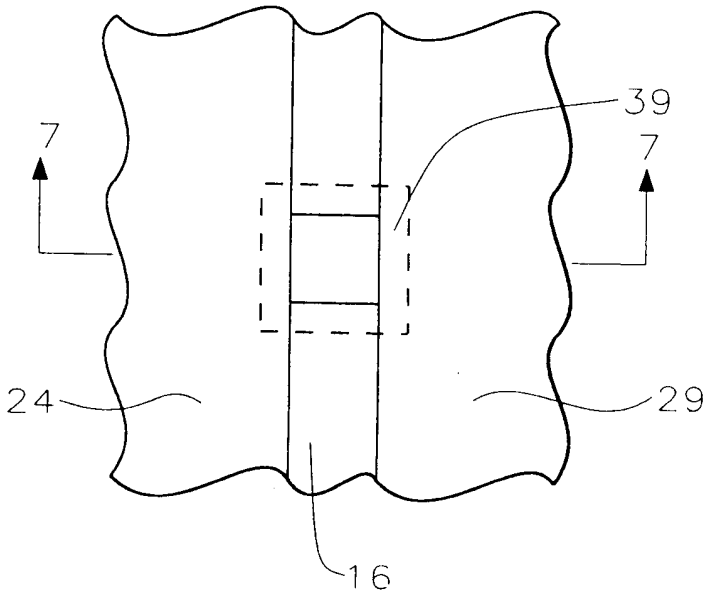

FIG. 8